those of FIG. **2** have been given similar identifying numerals. In FIG. **8***a*, however, the gate electrode is a polysilicon layer **101** (in place of aluminum) deposited atop gate oxide **25**. The gate **25** is then covered with oxide layer **102** and a conductive layer **103** connects the two sources **22** and **23** together to form a single source conductor which is insulated from gate **101**. Connection is made to the gate at some suitable edge portion of the wafer.

FIGS. **9** and **10** show the shape of measured curves which demonstrate the reduction in forward resistance when the region **40** is made highly conductive (n+). In FIG. **9**, the device tested had a region **40** which had the n(–) resistivity of the epitaxial region. Thus, the forward resistance is characteristically high at different gate biases as shown in FIG. **9**.

In the device of the invention where region **40** is of n(+) conductivity, there is a dramatic decrease in the on-resistance as shown in FIG. **10** for all gate voltages before velocity saturation of the electrons occurs.

Although the present invention has been described in connection with a preferred embodiment thereof, many variations and modifications will now become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

What is claimed is:

1. A three-terminal power metal oxide silicon field effect transistor device comprising:

a wafer of semiconductor material having first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of one conductivity type;

at least first and second spaced base regions of the opposite conductivity type to said one conductivity type formed in said wafer and extending from said first semiconductor surface to a depth beneath said first semiconductor surface; the space between said at least first and second base regions defining a common conduction region of one conductivity type at a given first semiconductor surface location;

first and second source regions of said one conductivity type formed in said at least first and second base regions, respectively, at first and second first surface locations and extending from said first and second first surface locations to a depth less than said depth of said base regions; said first and second source regions being laterally spaced along said first semiconductor surface from the facing respective edges of said common conduction region thereby to define first and second channel regions along said first semiconductor surface between each of said first and second source regions, respectively, and said common conduction region;

source electrode means connected to said source regions and comprising a first terminal;

gate insulation layer means on said first surface, disposed at least on said first and second channel regions;

gate electrode means on said gate insulation layer means, overlying said first and second channel regions and comprising a second terminal;

a drain electrode connected to said first surface and comprising a third terminal;

each of said at least first and second spaced base regions of said opposite conductivity type having respective profiles which include relatively shallow depth regions extending from said common region and underlying their said respective first and second source regions, and respective relatively deep, relatively large radius regions extending from said shallow depth regions which are laterally spaced from beneath said respective source regions on the side of said source regions which is away from said common region.

2. The device of claim **1**, wherein said device is formed by DMOS manufacturing techniques.

3. The device of claim **1**, wherein said gate insulation layer means is silicon dioxide.

4. The device of claim **1**, wherein said one conductivity type is n-type and wherein said opposite conductivity type is p-type.

5. The device of claim **1**, wherein said gate electrode means is formed of polysilicon.

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